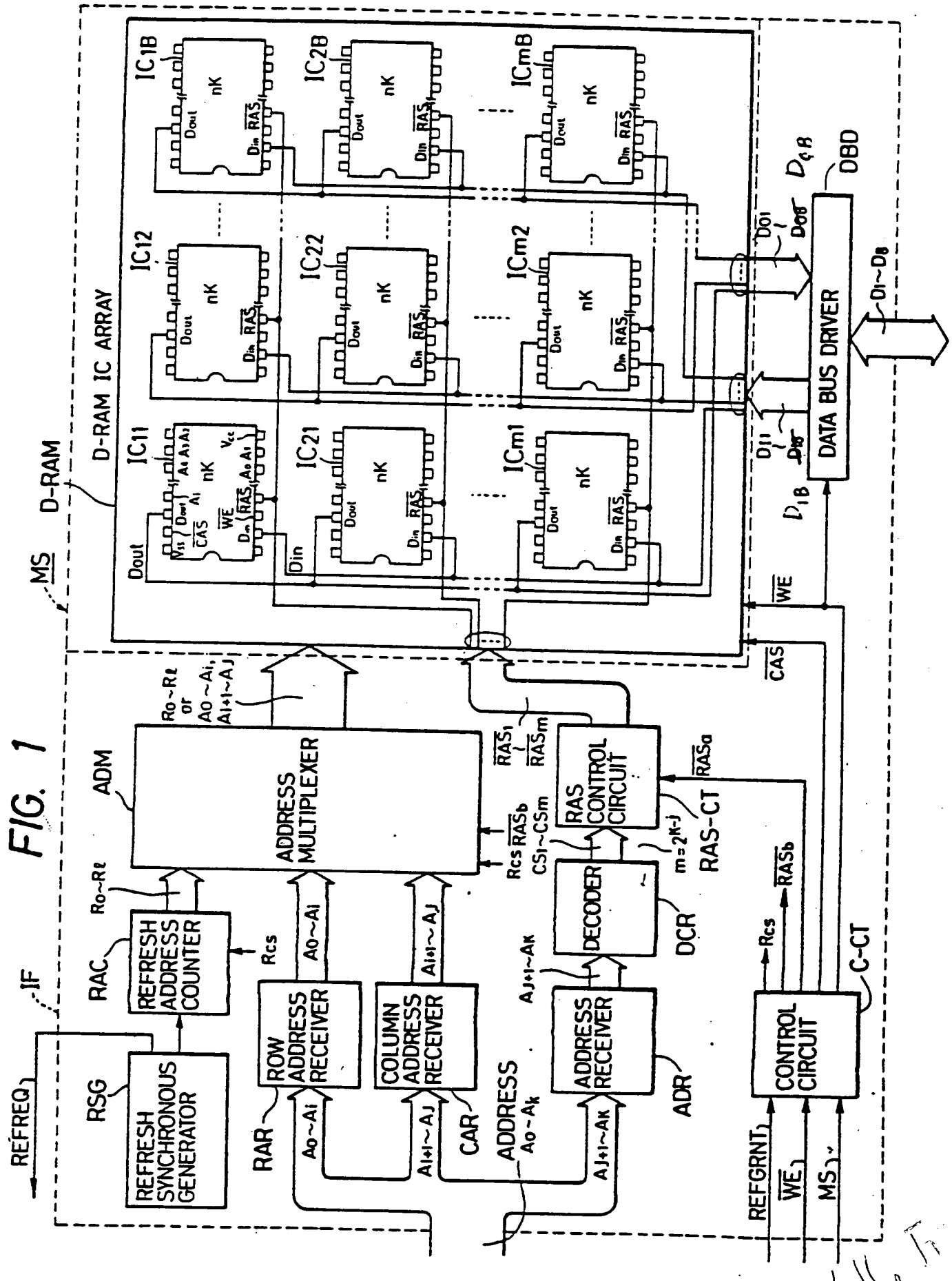

D-RAM
D-RAM IC ARRAY
IC11
IC12
IC1B
IC21
IC22
IC2B
ICm1
ICm2
ICmB
nK
Dout
Din
RAS
CAS
WE
DATA BUS DRIVER
DBD
D1~DB
ADM
ADDRESS MULTIPLEXER
RAS CONTROL CIRCUIT
RAS-CT
DECODER
DCR
REFRESH ADDRESS COUNTER
RAC
ROW ADDRESS RECEIVER
RAR
COLUMN ADDRESS RECEIVER
CAR
ADDRESS RECEIVER
ADR
ADDRESS
CONTROL CIRCUIT
C-CT
REFRESH SYNCHRONOUS GENERATOR
RSG
REFREQ
REFGRNT
IF
MS

FIG. 1

FIG. 2

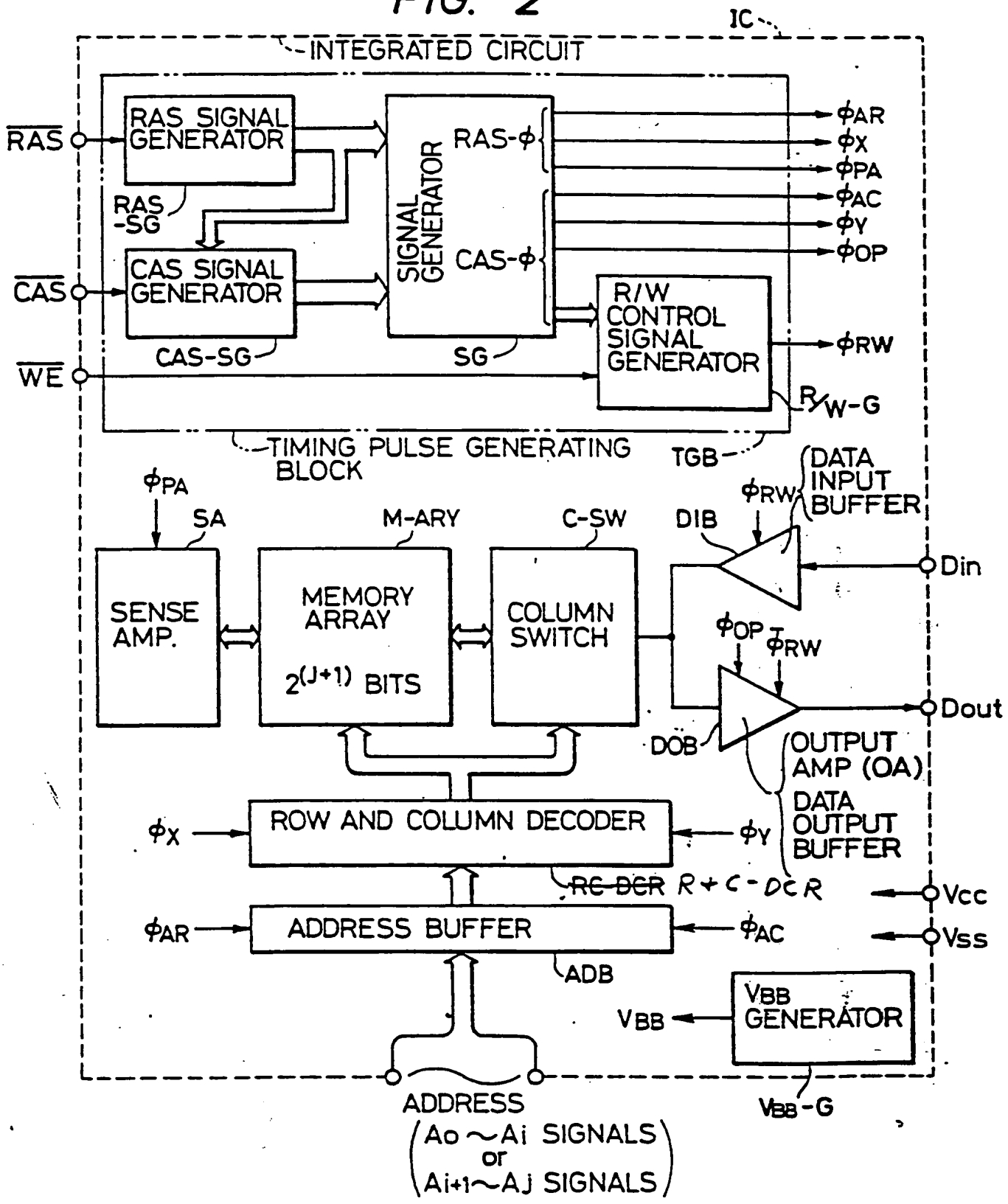
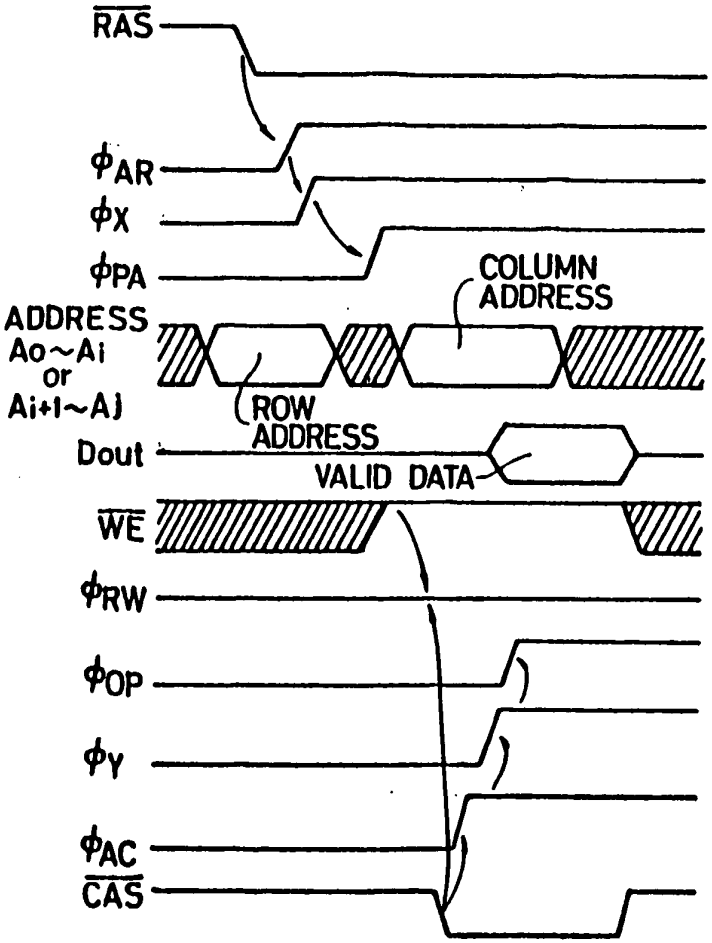
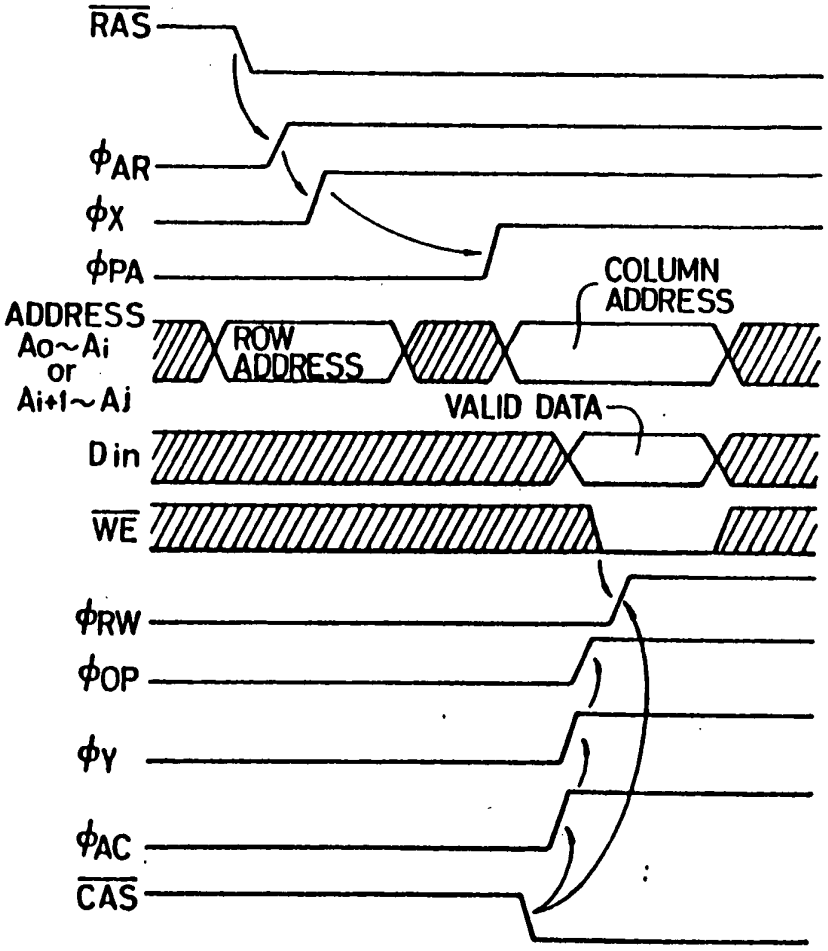

IC
INTEGRATED CIRCUIT
RAS
RAS SIGNAL GENERATOR
RAS -SG
CAS
CAS SIGNAL GENERATOR
CAS-SG
WE
SIGNAL GENERATOR
RAS-φ
CAS-φ
SG
R/W CONTROL SIGNAL GENERATOR
φAR
φX
φPA
φAC
φY
φOP
φRW
R/W-G
TIMING PULSE GENERATING BLOCK
TGB
φPA
SA
M-ARY
C-SW
DIB
φRW
DATA INPUT BUFFER
Din
SENSE AMP.
MEMORY ARRAY
2(J+1) BITS
COLUMN SWITCH
φOP
φRW
Dout
DOB
OUTPUT AMP (OA)
DATA OUTPUT BUFFER
φX
ROW AND COLUMN DECODER
φY
RC-DCR
R+C-DCR
Vcc
φAR
ADDRESS BUFFER
φAC
Vss
ADB
VBB
VBB GENERATOR
VBB-G
ADDRESS
(Ao ~ Ai SIGNALS or Ai+1 ~ Aj SIGNALS)

FIG. 3A



〈READ CYCLE〉

FIG. 3B



〈WRITE CYCLE〉

FIG. 4A

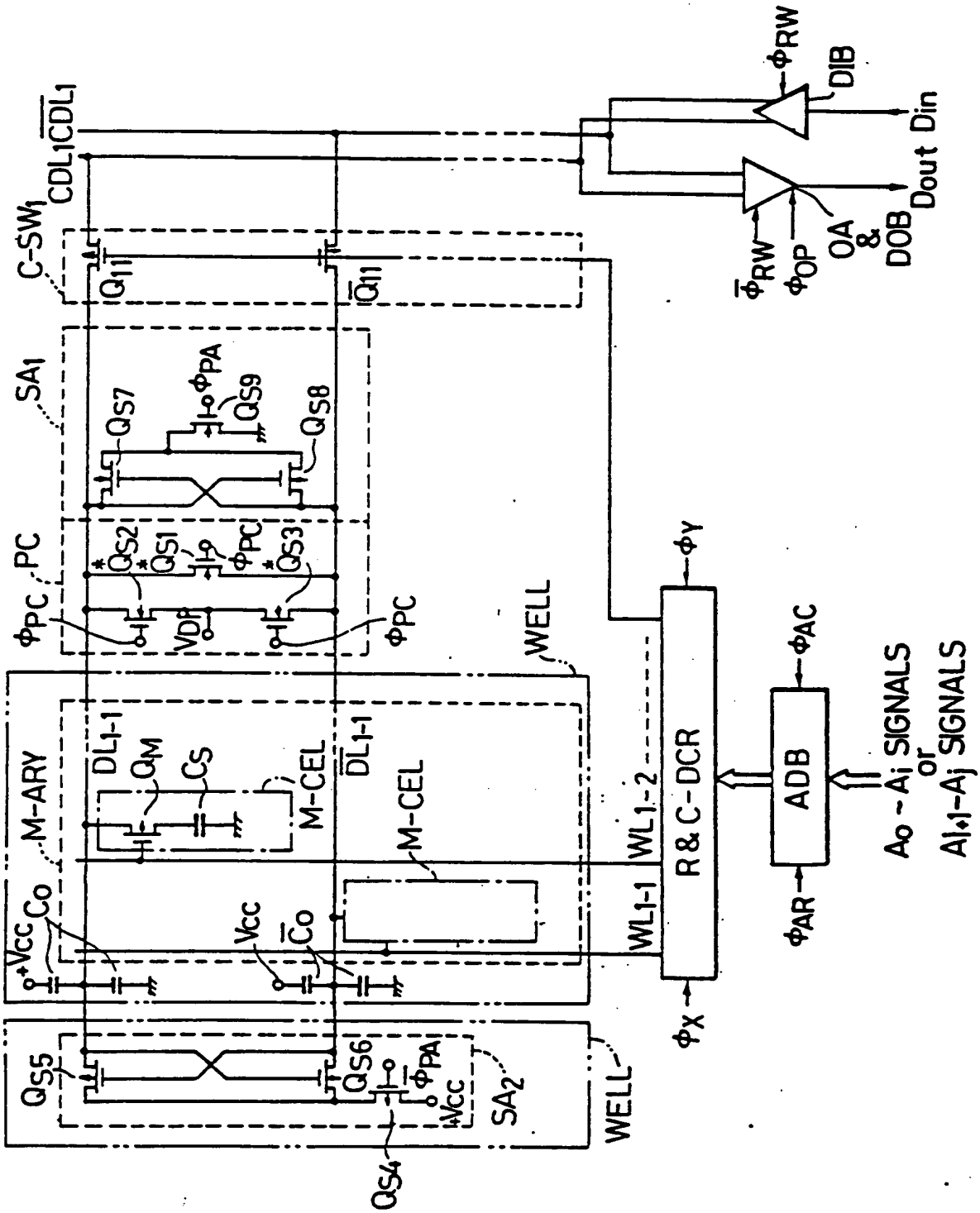

M-ARY
M-CEL
M-CEL
WELL
WELL
SA1
SA2
C-SW1
PC
R & C-DCR
ADB
WL1-1
WL1-2
DIB
Din
Dout
OA & DOB
Ao - Ai SIGNALS or Ai+1 - Aj SIGNALS

FIG. 4B

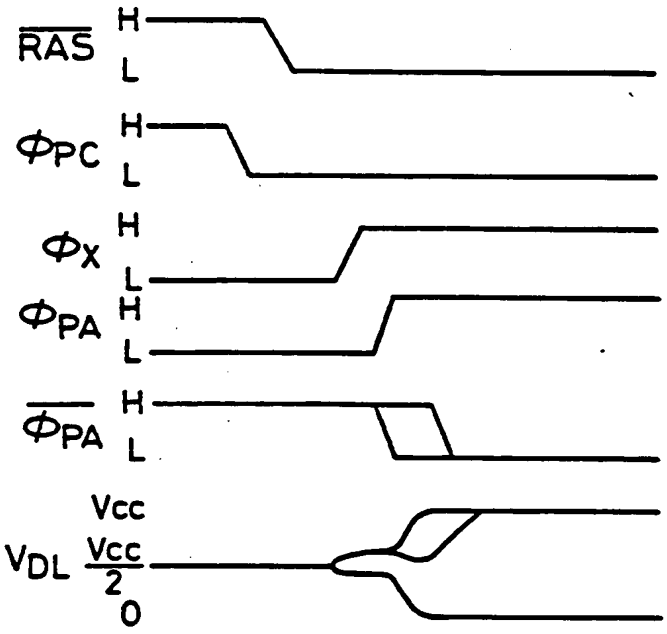

$\overline{RAS}$
H
L
Φ_{PC}
H
L
Φ_X
H
L
Φ_{PA}
H
L
$\overline{\Phi_{PA}}$
H
L
Vcc
V_{DL}
Vcc
2
0

FIG. 4D

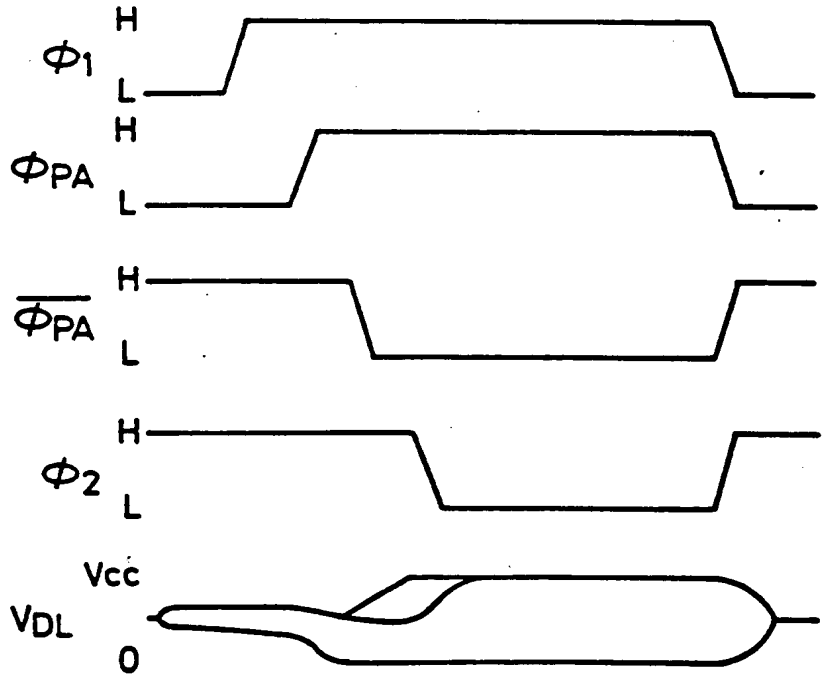

Φ_1
H
L
Φ_{PA}
H
L
$\overline{\Phi_{PA}}$
H
L
Φ_2
H
L
Vcc
V_{DL}
0

FIG. 4C

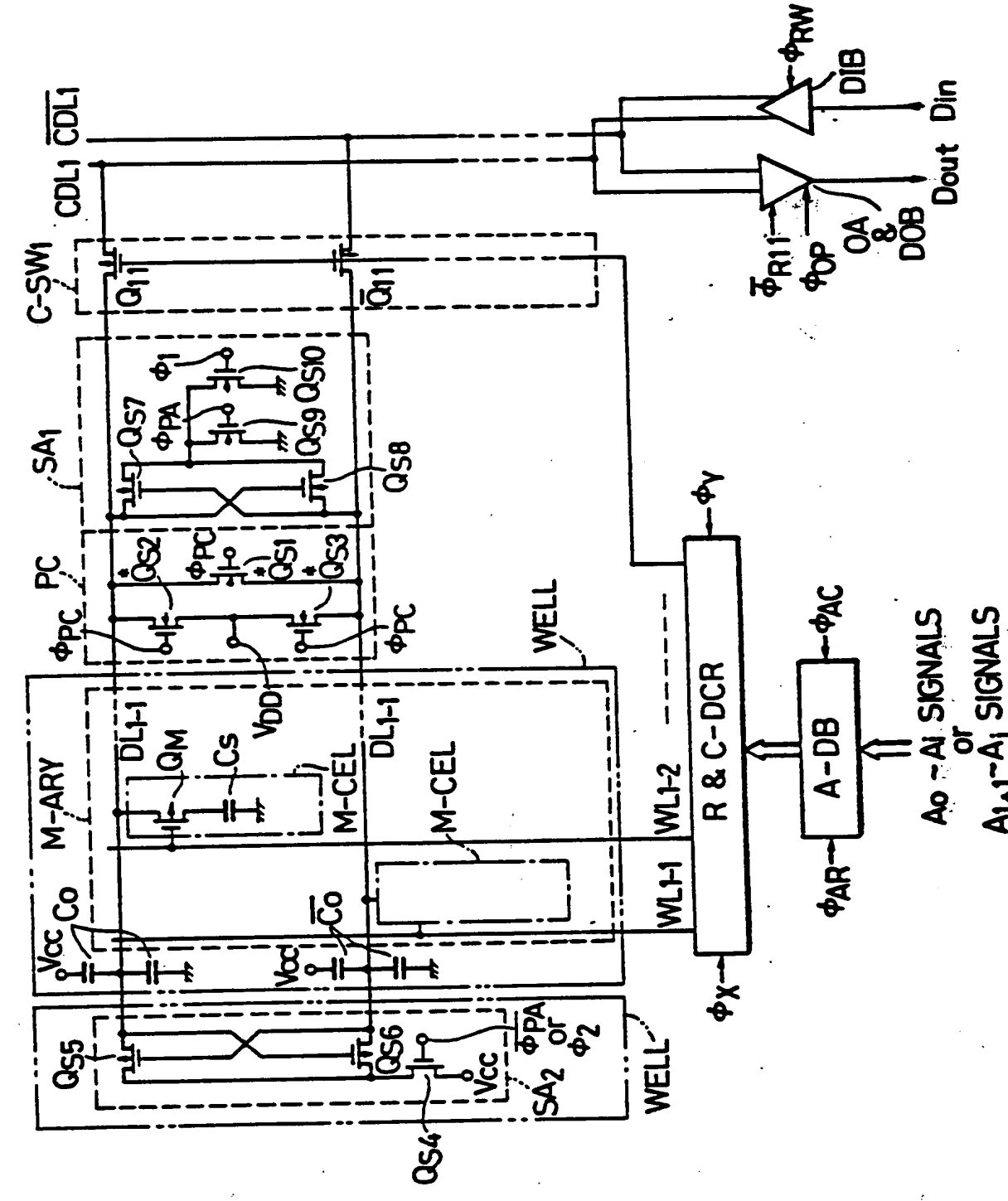

M-ARY
M-CEL
DL1-1
WL1-1
WL1-2
WELL
R & C-DCR
A-DB
C-SW1
SA1
SA2
PC
CDL1
DIB
Din
Dout
OA & DOB
Ao ~Ai SIGNALS or Ai+1~Aj SIGNALS

FIG. 4E

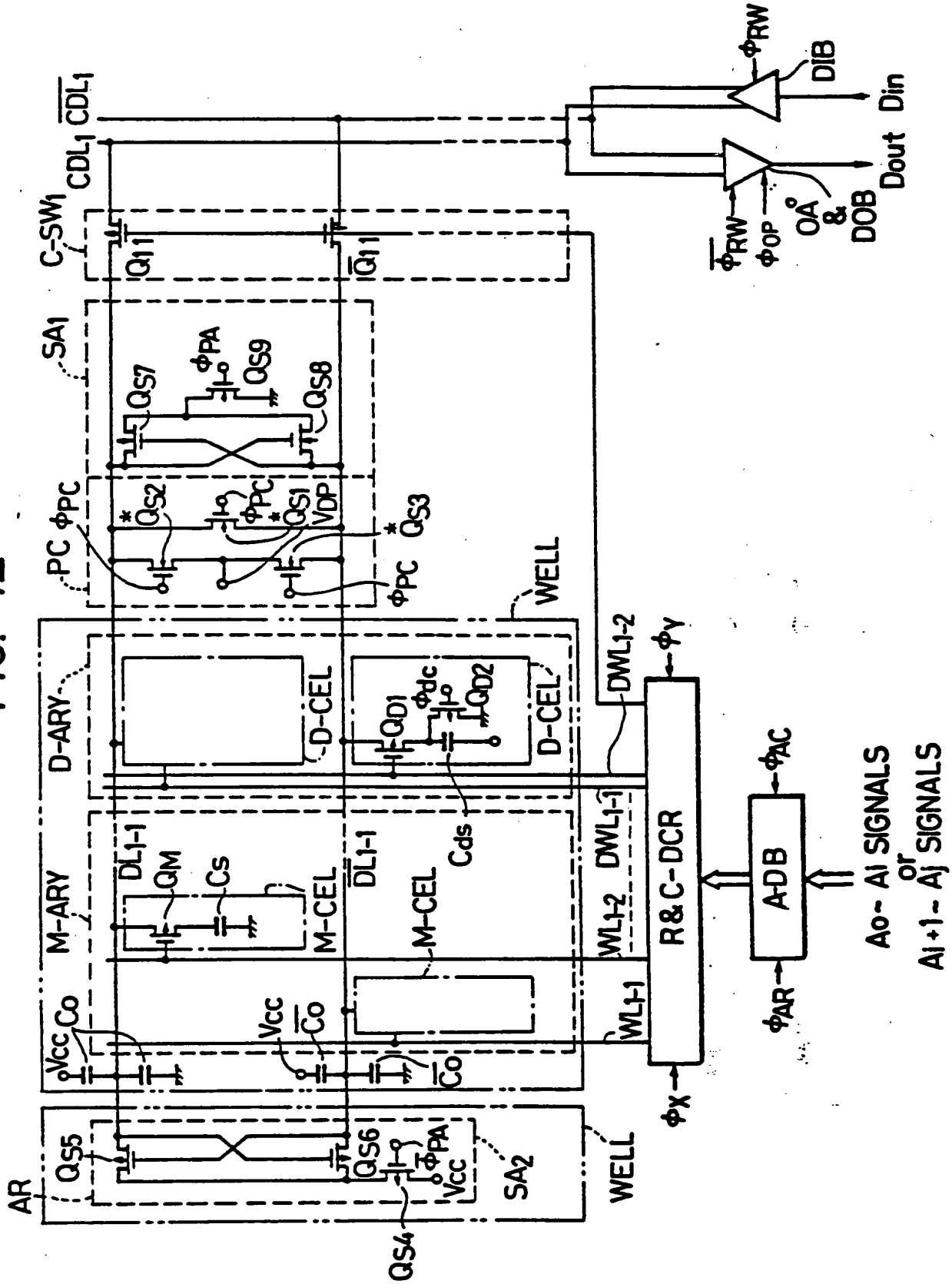

AR
M-ARY
D-ARY
SA1
SA2
C-SW
PC
WELL
WELL
D-CEL
D-CEL
M-CEL
M-CEL
DL1-1
DL1-1
DWL1-2
DWL1-1
WL1-2
WL1-1
R&C-DCR
A-DB
Ao~ Ai SIGNALS
or
Ai+1~ Aj SIGNALS
DIB
Din
Dout
DOB
OA
Vcc
Co
Cs
Cds
QM
QD1
QD2
QS1
QS2
QS3
QS4
QS5
QS6
QS7
QS8
QS9
Q11
VDP

FIG. 5A

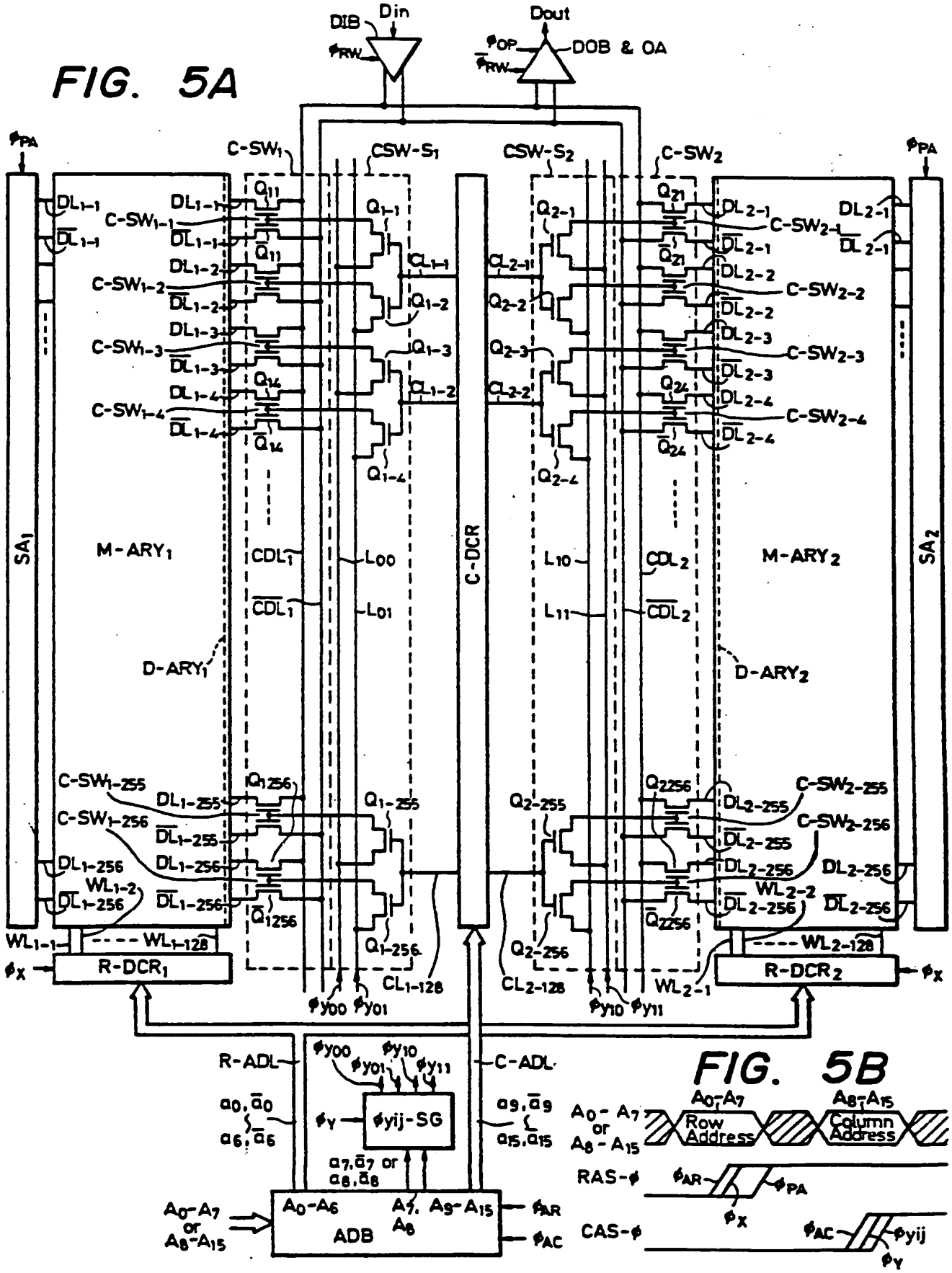

DIB
Din
Dout
DOB & OA
C-SW1
CSW-S1
CSW-S2
C-SW2
SA1
SA2
M-ARY1
M-ARY2
C-DCR
CDL1
CDL2
D-ARY1
D-ARY2
R-DCR1
R-DCR2
R-ADL
C-ADL
ADB
Row Address
Column Address
RAS-φ
CAS-φ

FIG. 5B

FIG. 6

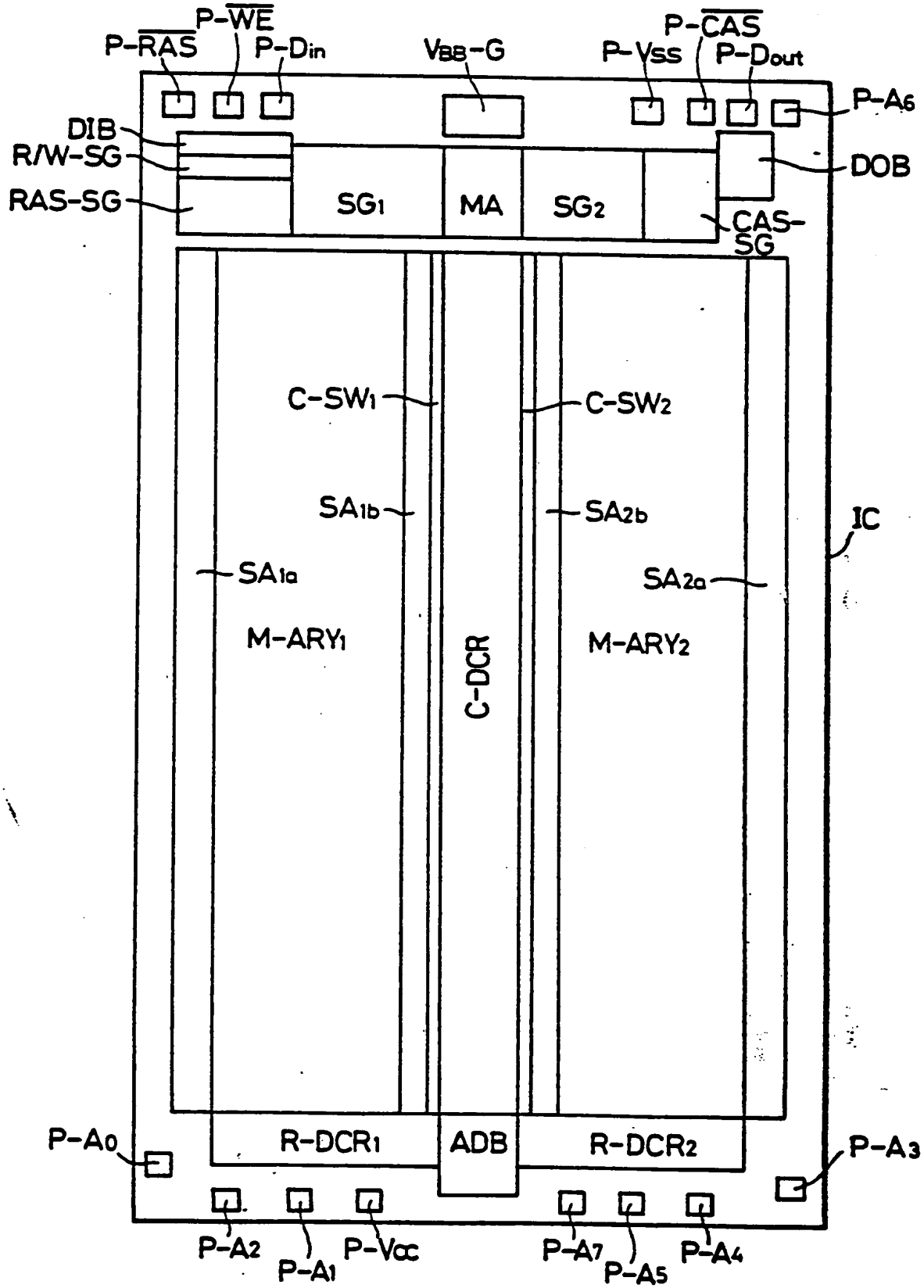

P-RAS
P-WE
P-Din
VBB-G
P-Vss
P-CAS
P-Dout
P-A6
DIB
R/W-SG
RAS-SG
SG1
MA
SG2
DOB
CAS-SG
C-SW1
C-SW2
SA1b
SA2b
IC
SA1a
SA2a
M-ARY1
M-ARY2
C-DCR
P-A0
R-DCR1
ADB
R-DCR2
P-A3
P-A2
P-A1
P-Vcc
P-A7
P-A5
P-A4

FIG. 7A

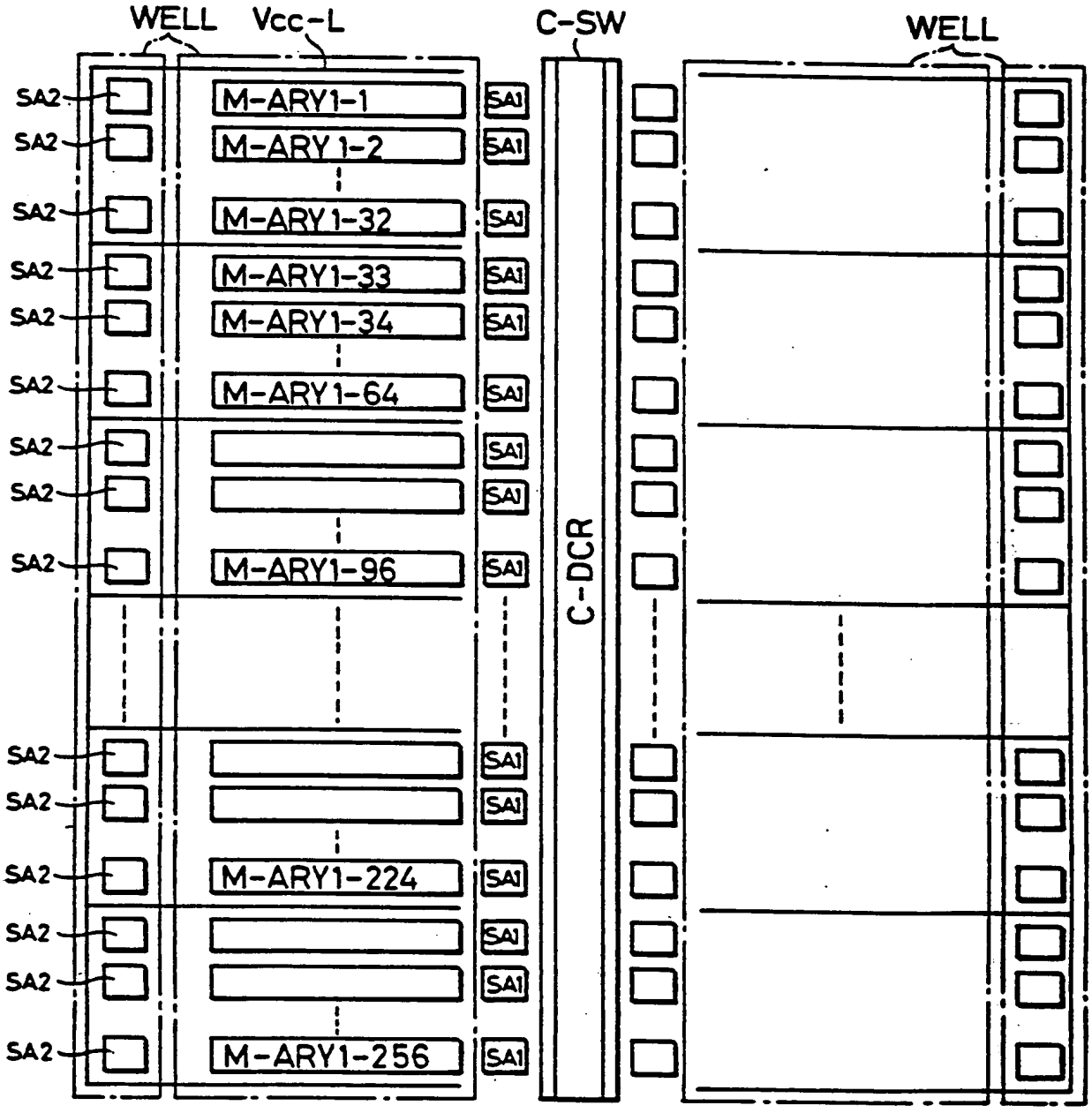

WELL
Vcc-L
C-SW
WELL
C-DCR
SA2
SA1
M-ARY1-1
M-ARY1-2
M-ARY1-32
M-ARY1-33
M-ARY1-34
M-ARY1-64
M-ARY1-96
M-ARY1-224
M-ARY1-256

FIG. 7B

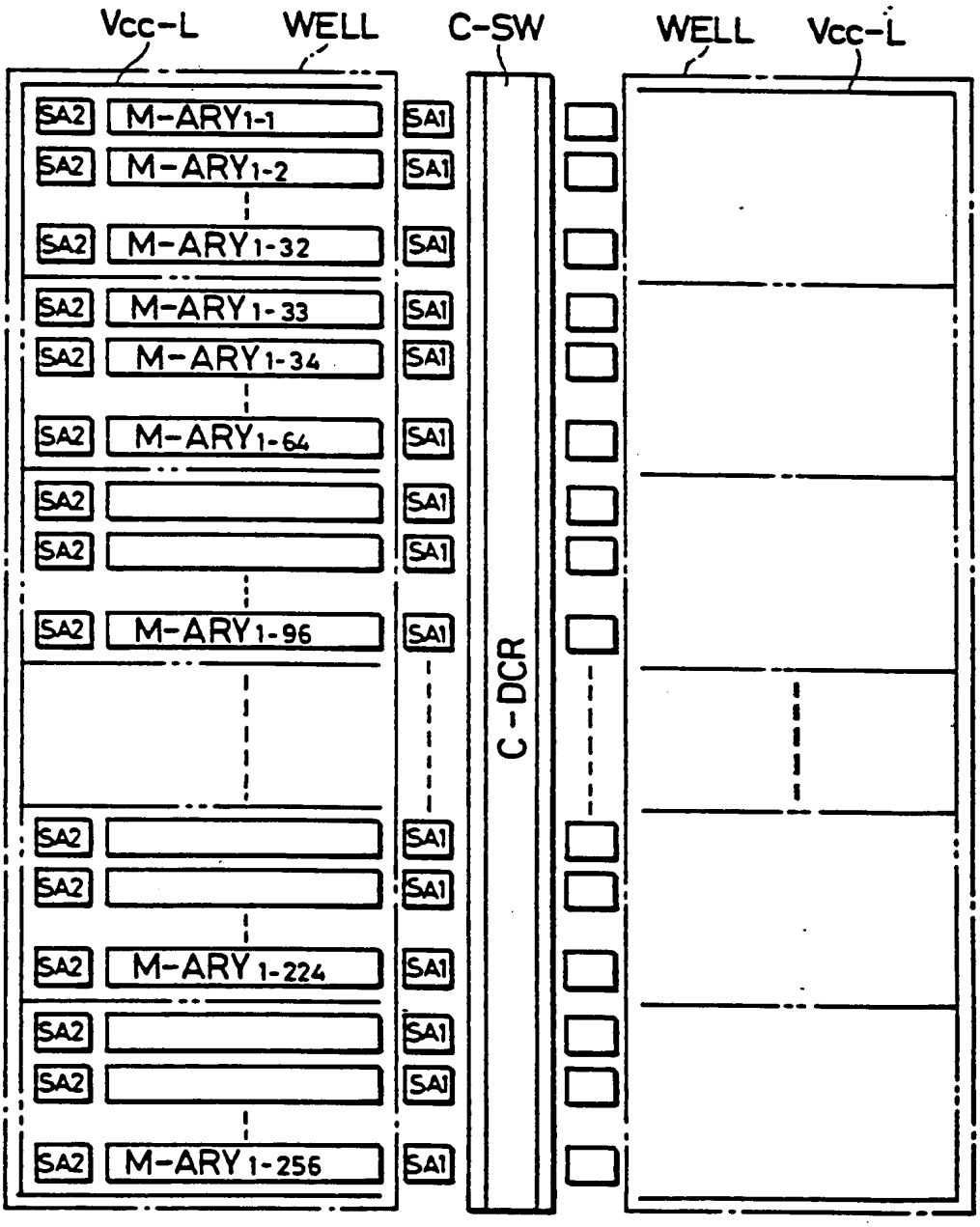

Vcc-L
WELL
C-SW
WELL
Vcc-L
SA2
M-ARY1-1
SA1
M-ARY1-2
M-ARY1-32
M-ARY1-33
M-ARY1-34
M-ARY1-64
M-ARY1-96
M-ARY1-224
M-ARY1-256
C-DCR

FIG. 8A

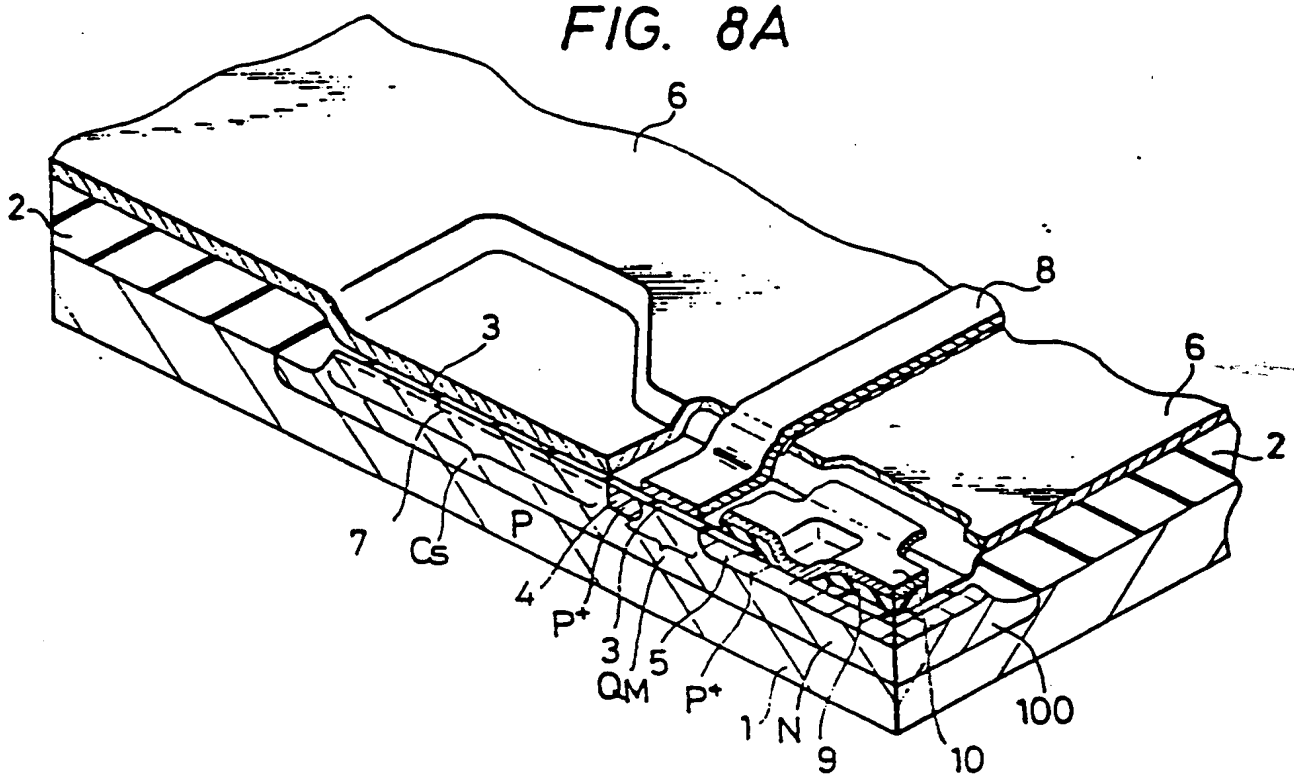

6
2
8
3
6
2
7
Cs
P
4
P+
3
5
QM
P+
1
N
9
10
100

FIG. 8B

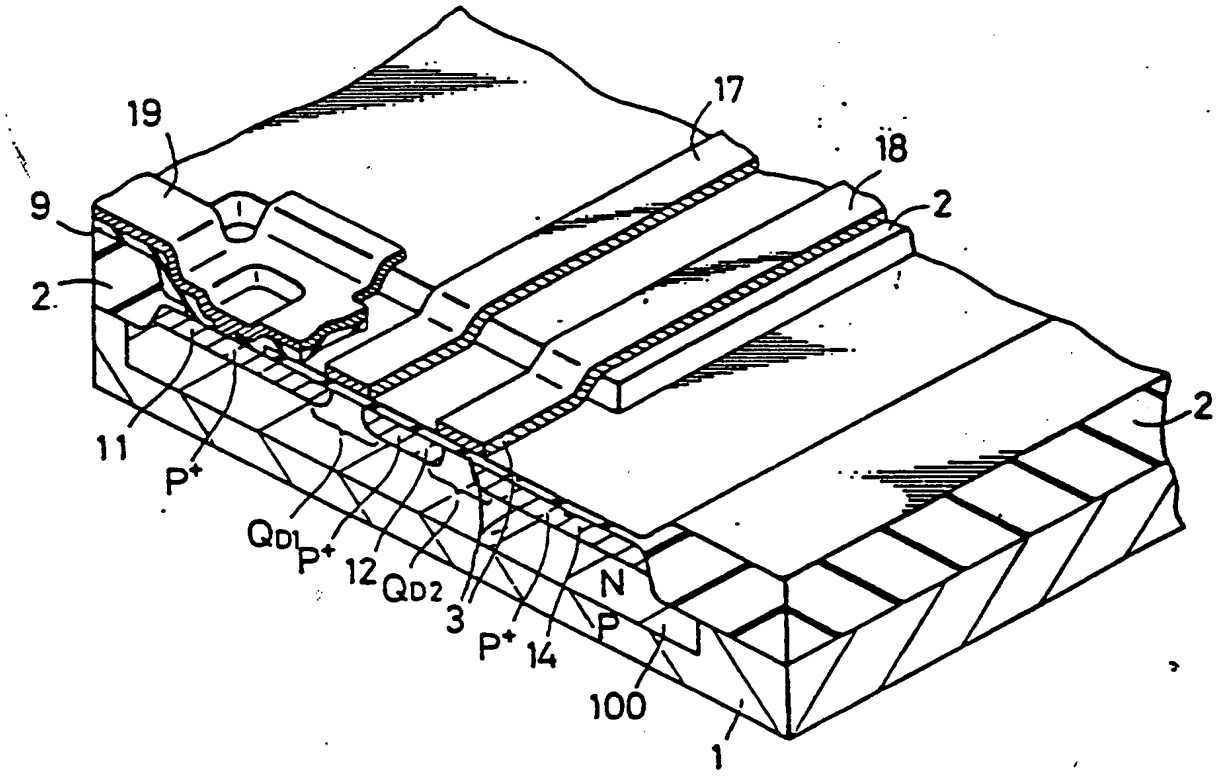

19
17
18
9
2
2
2
11
P+
QD1
P+
12
QD2
3
P+
14
N
P
100
1

FIG. 9A

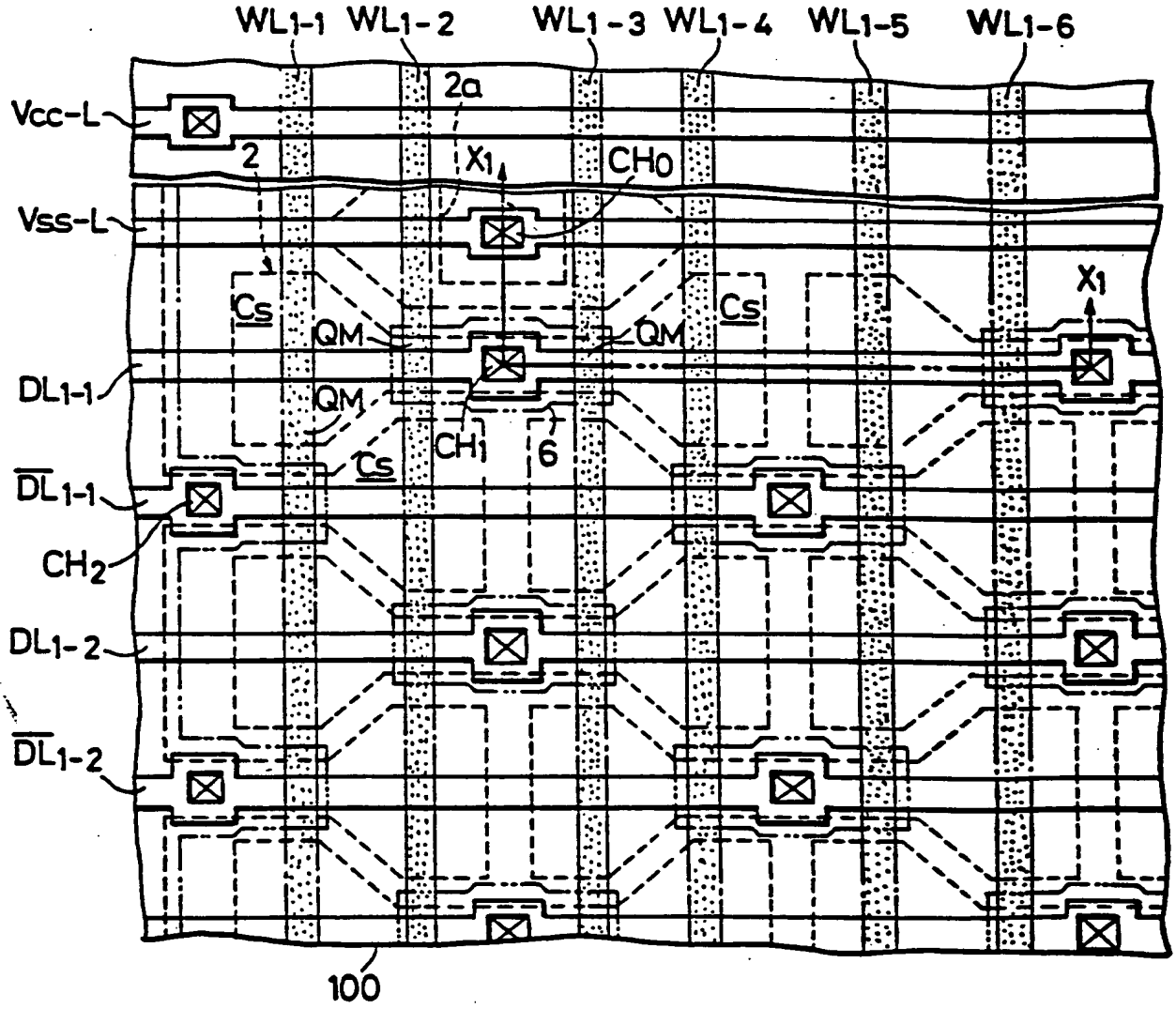

WL1-1
WL1-2
WL1-3
WL1-4
WL1-5
WL1-6
Vcc-L
Vss-L
DL1-1
DL1-1
DL1-2
DL1-2
2
2a
X1
CH0
Cs
QM
CH1
6
CH2
100

FIG. 9B

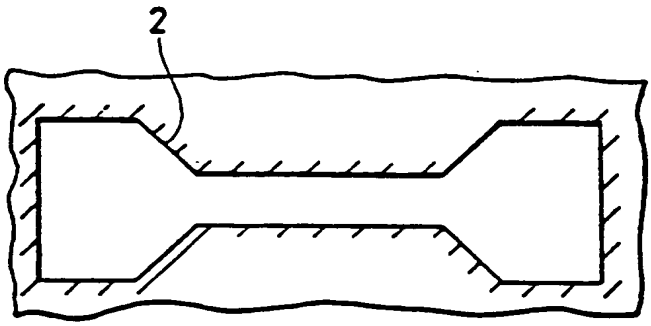


FIG. 9C

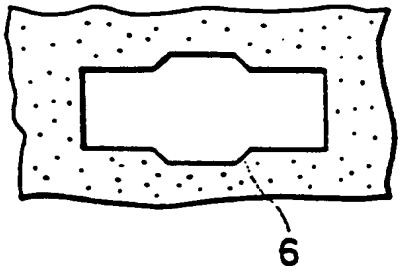
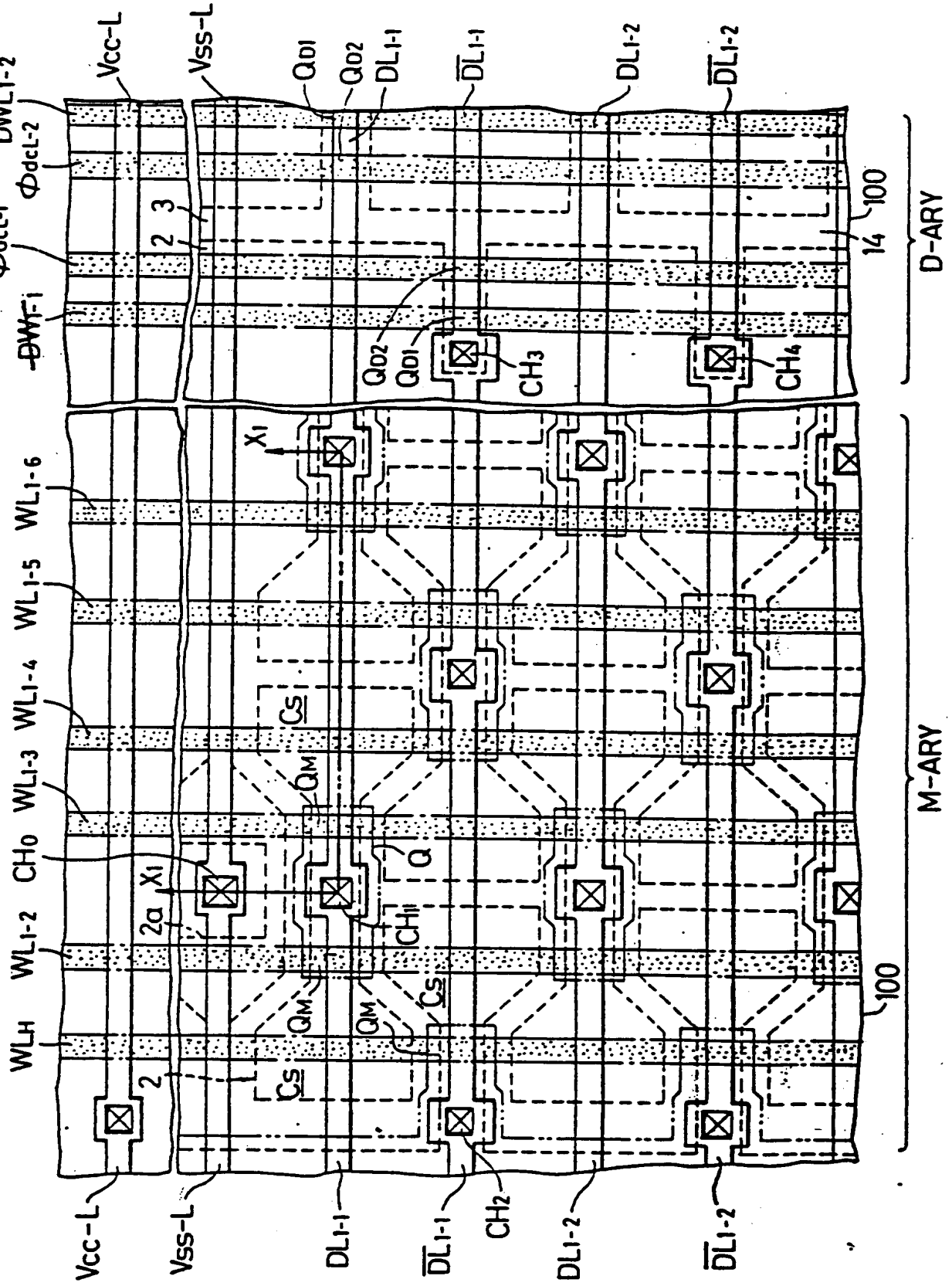


FIG. 9D


Vcc-L
Vss-L
QD1
QD2
DL1-1
DL1-1
DL1-2
DL1-2
DWL1-2
ΦdCL-2
ΦdCL-1
DWL1-1
DWL1-1
2 3
QD2
QD1
CH3
CH4
14
100
D-ARY
X1
WL1-6
WL1-5
WL1-4
WL1-3
WL1-2
WLH
CH0
2a
X1
CS
QM
Q
CH1
CS
QM
QM
CS
2
100
M-ARY
Vcc-L
Vss-L
DL1-1
DL1-1
CH2
DL1-2
DL1-2

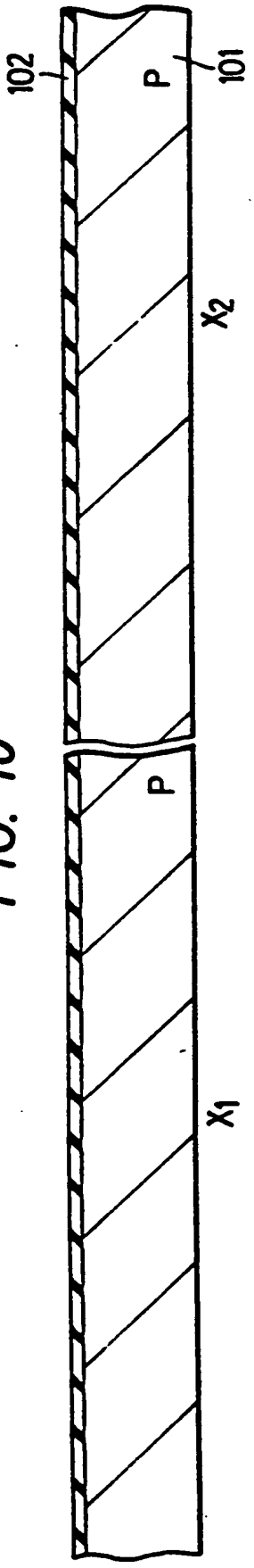


FIG. 10

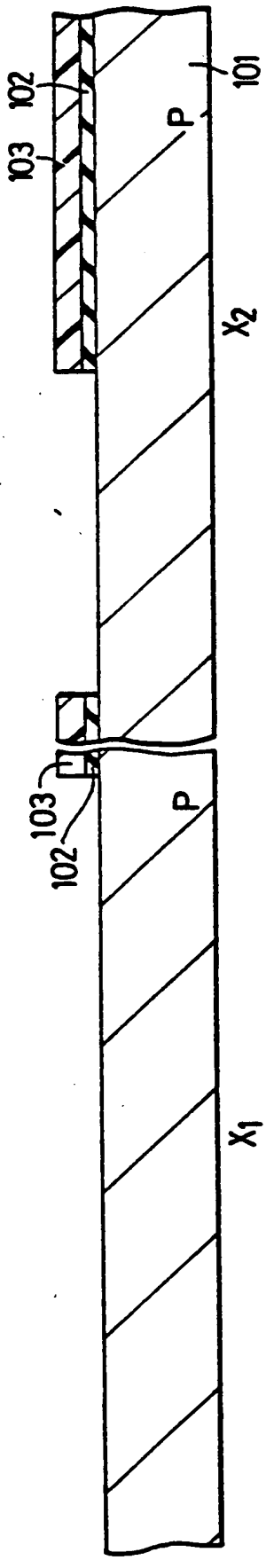


FIG. 11

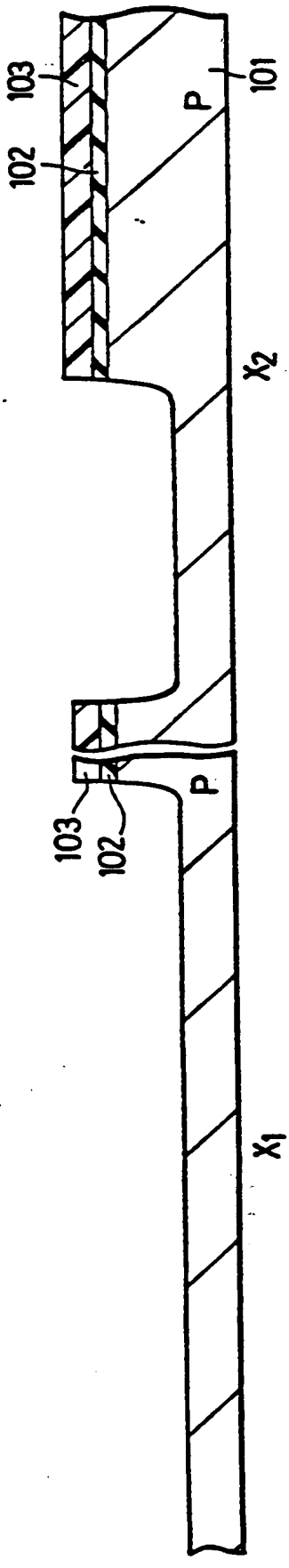


FIG. 12

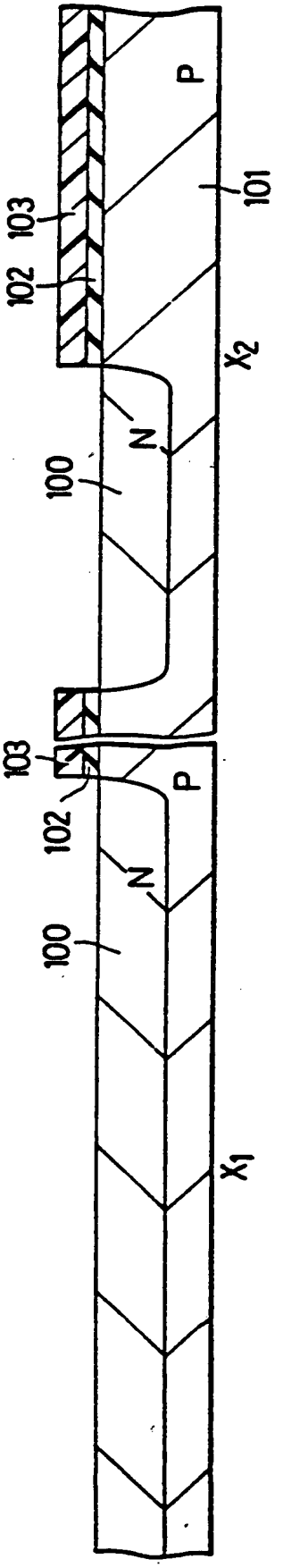


FIG. 13

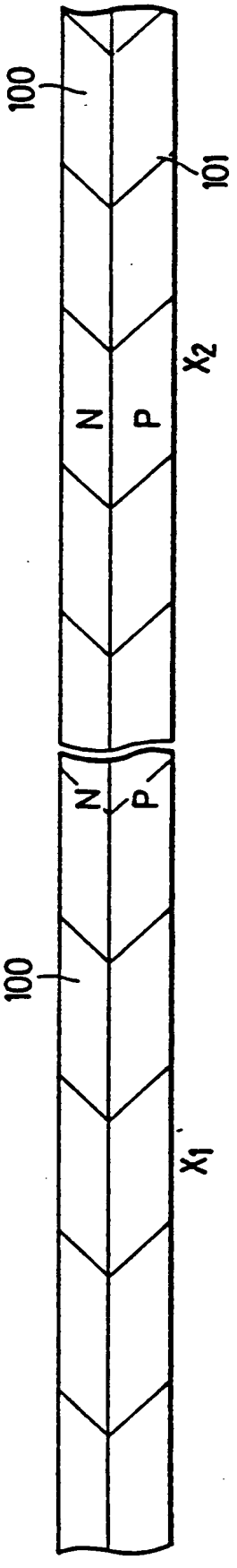


FIG. 14

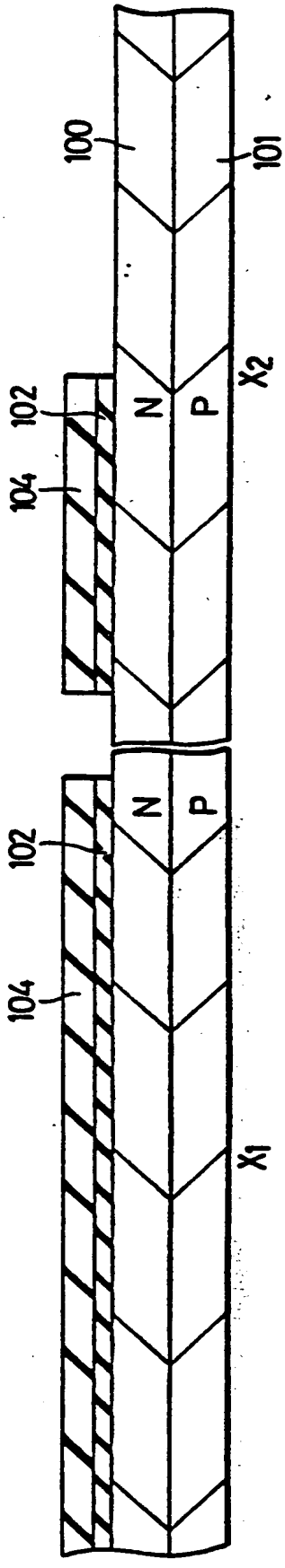


FIG. 15

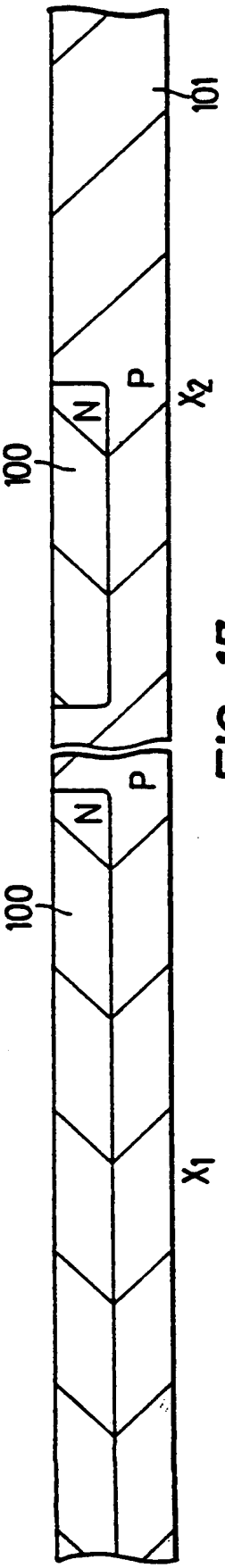


FIG. 16

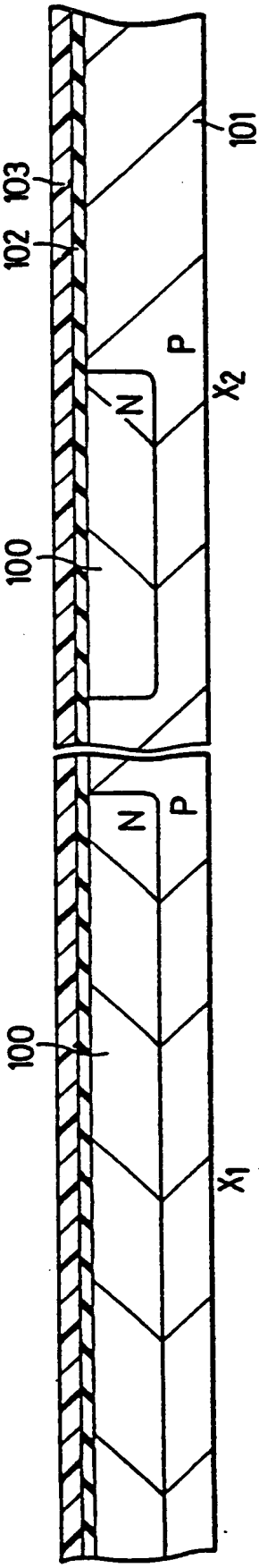


FIG. 17

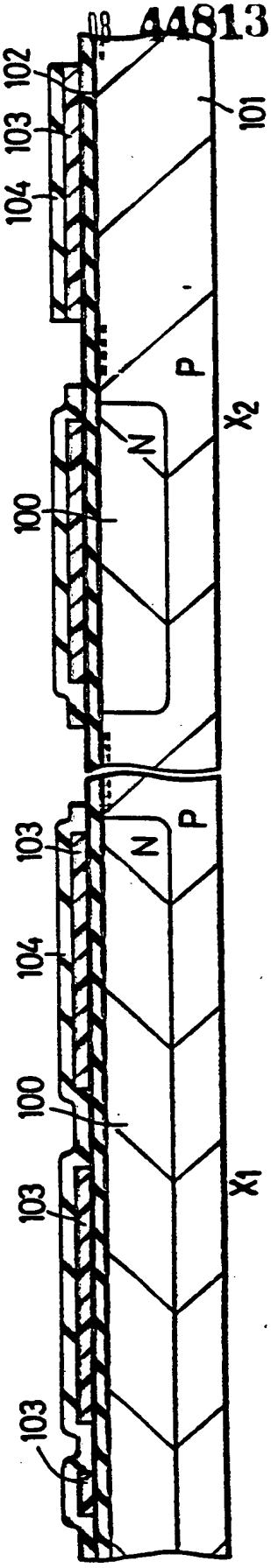


FIG. 18

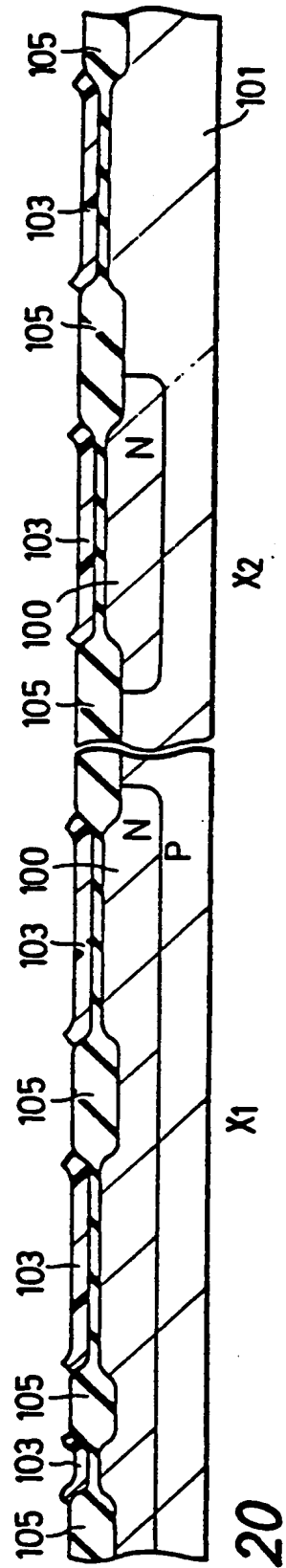

105
103
105
103
100
105
N
P
N
103
100
103
105
103
105
105
101
X2
X1

FIG. 19

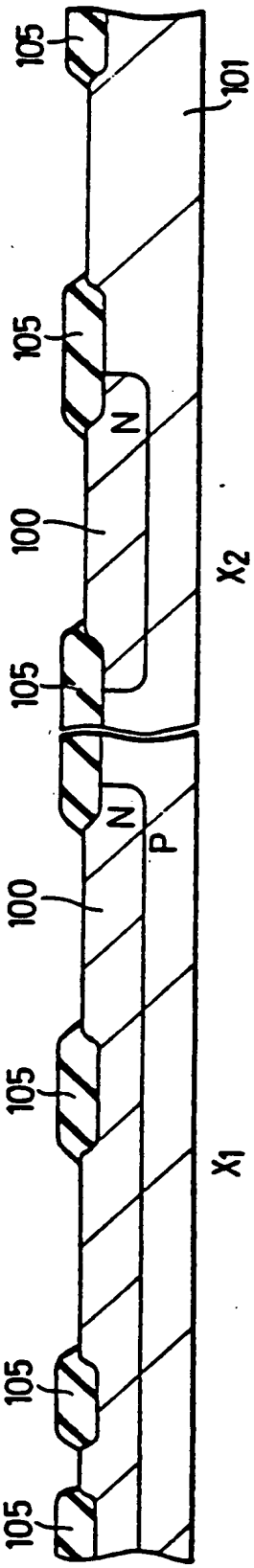

105
105
N
100
105
N
P
N
100
105
105
105
101
X2
X1

FIG. 20

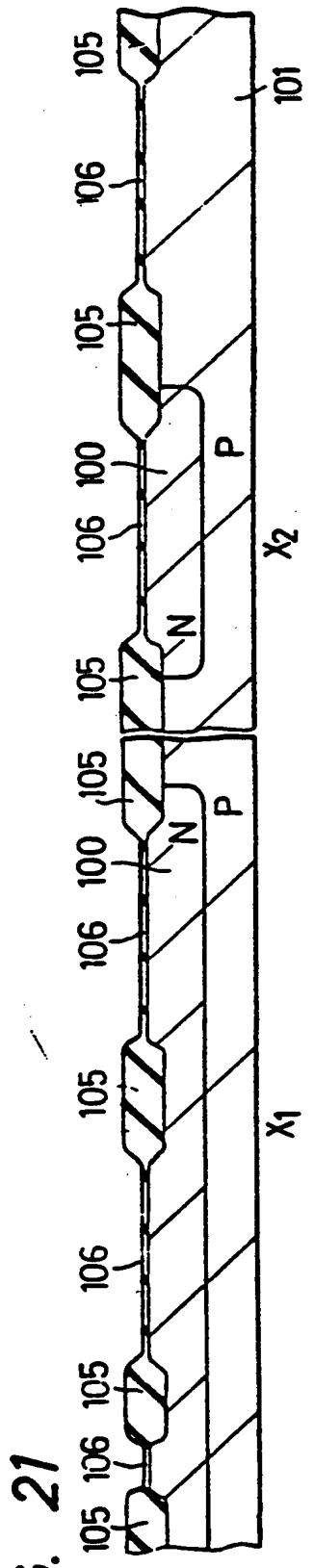


FIG. 21

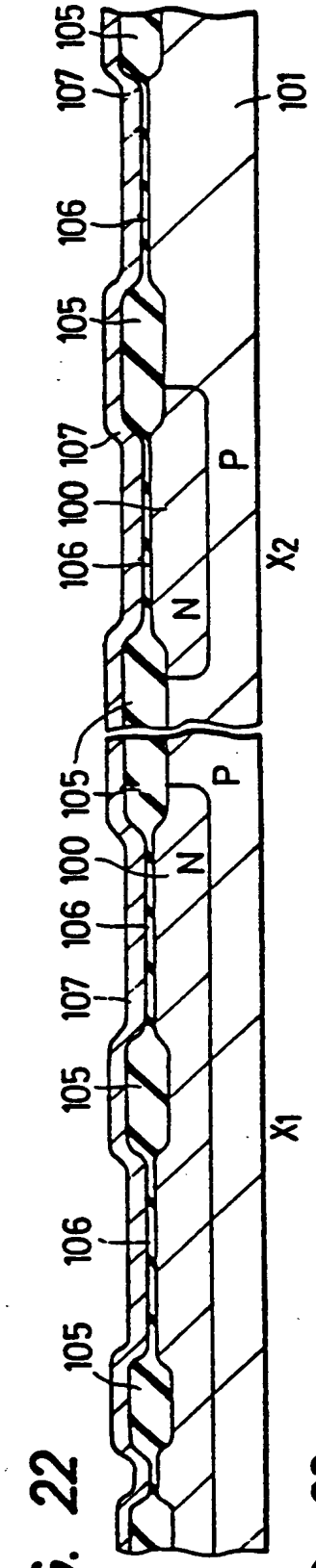


FIG. 22

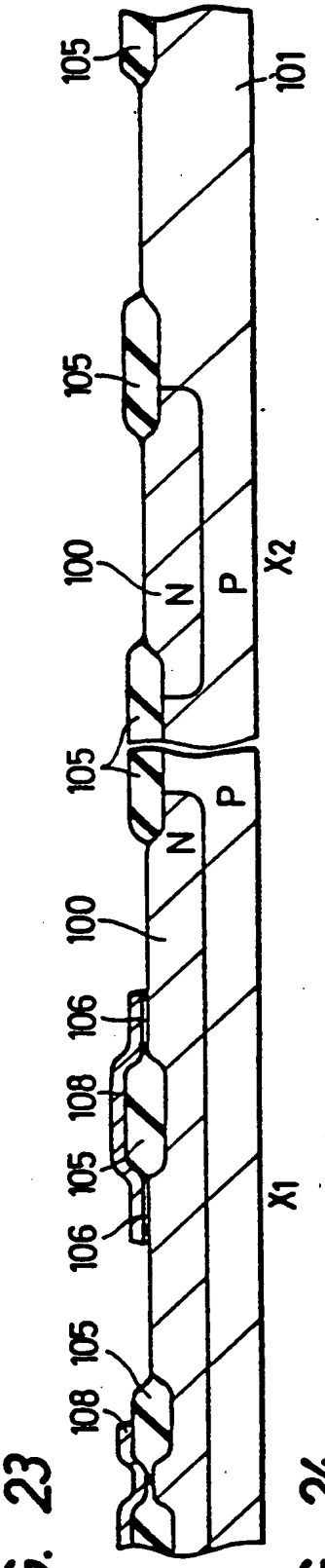


FIG. 23

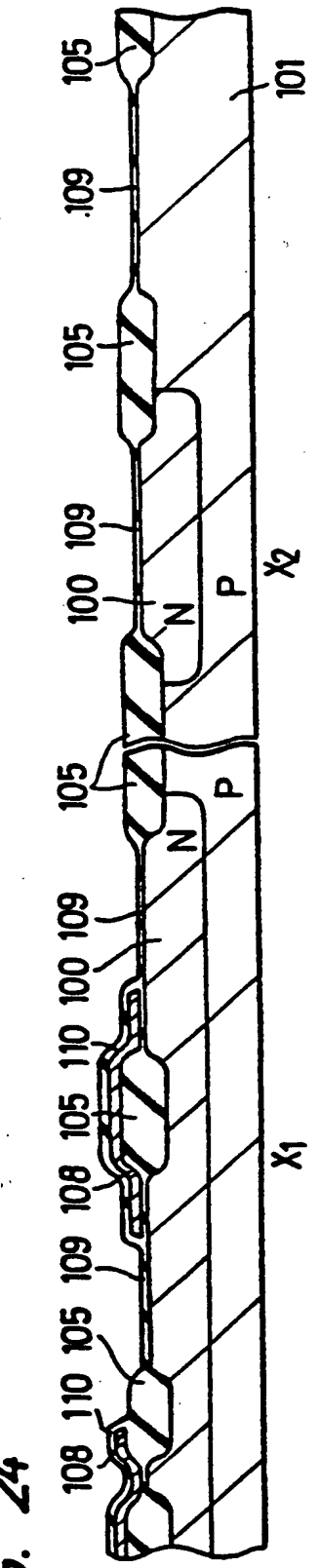


FIG. 24

FIG. 25

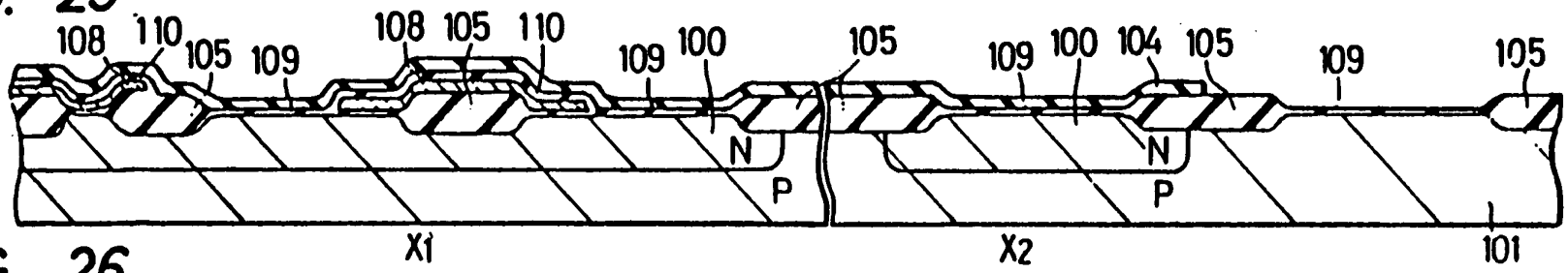


FIG. 26

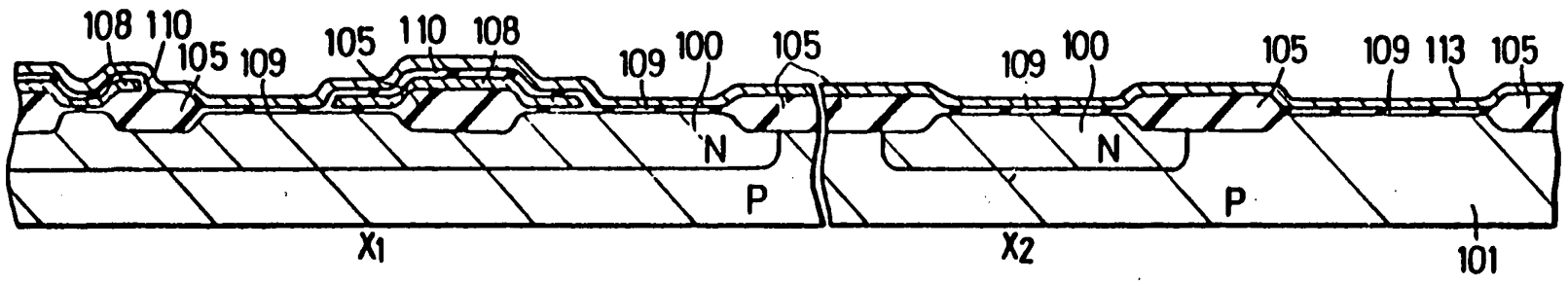


FIG. 27

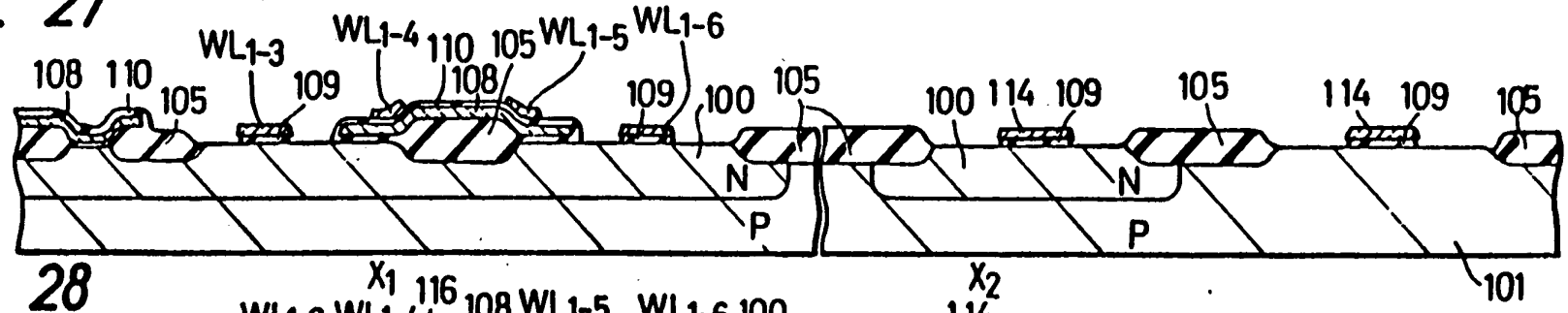


FIG. 28

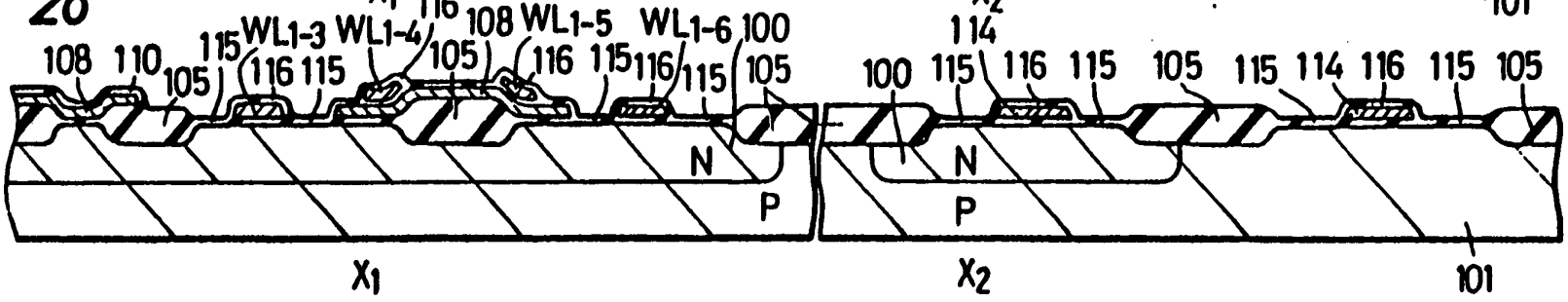


FIG. 29

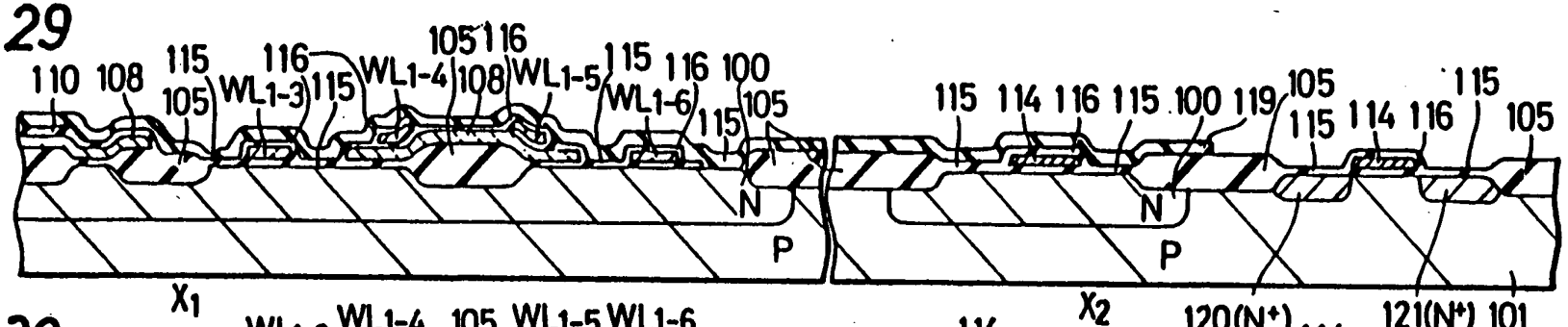


FIG. 30

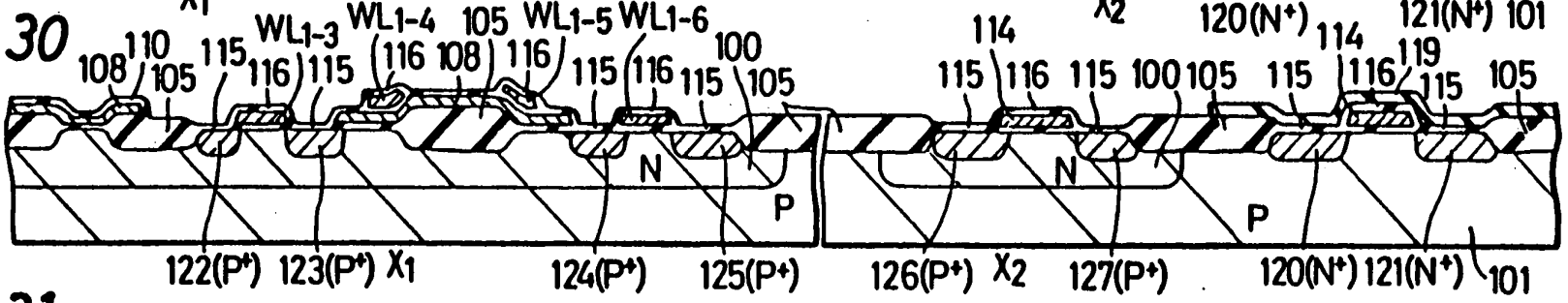


FIG. 31

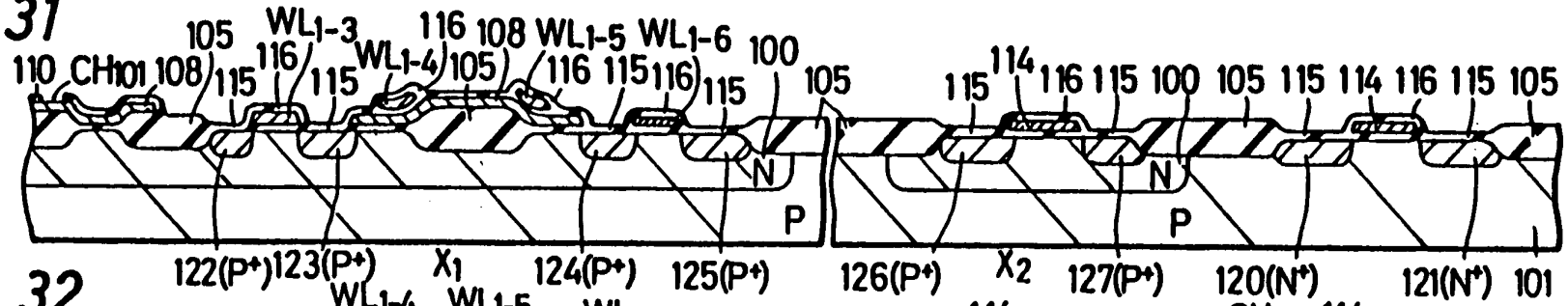


FIG. 32

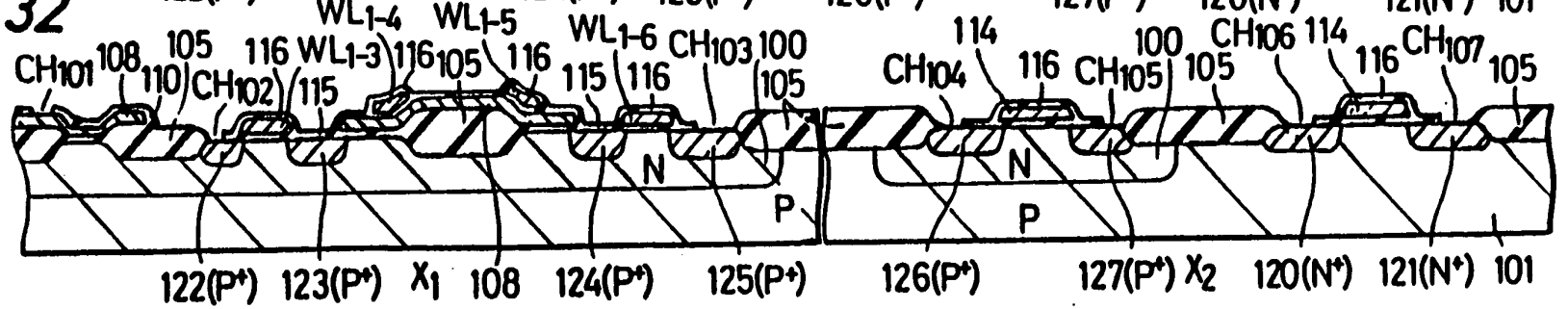


FIG. 33

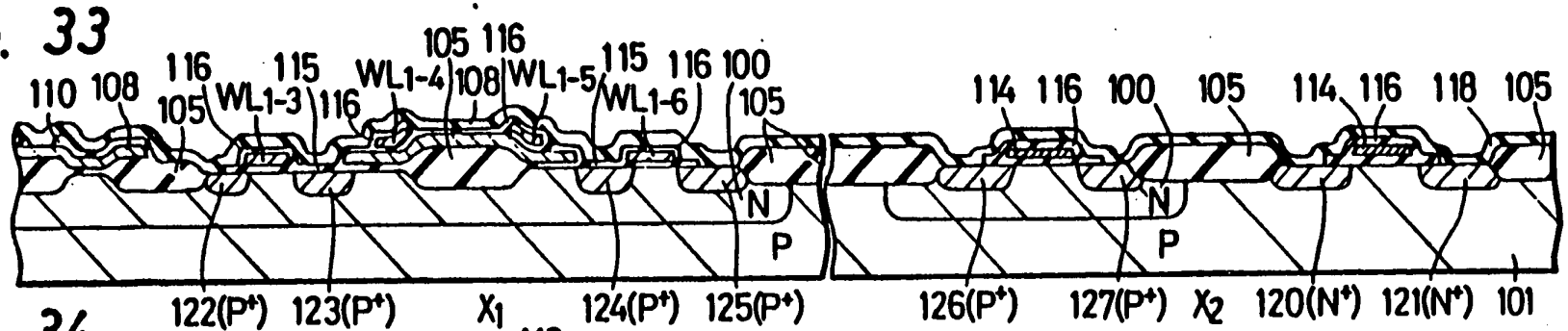


FIG. 34

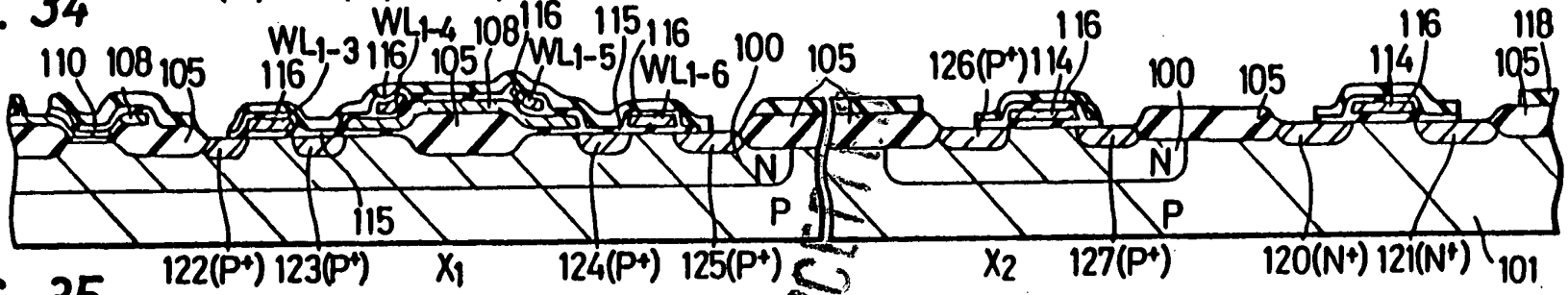
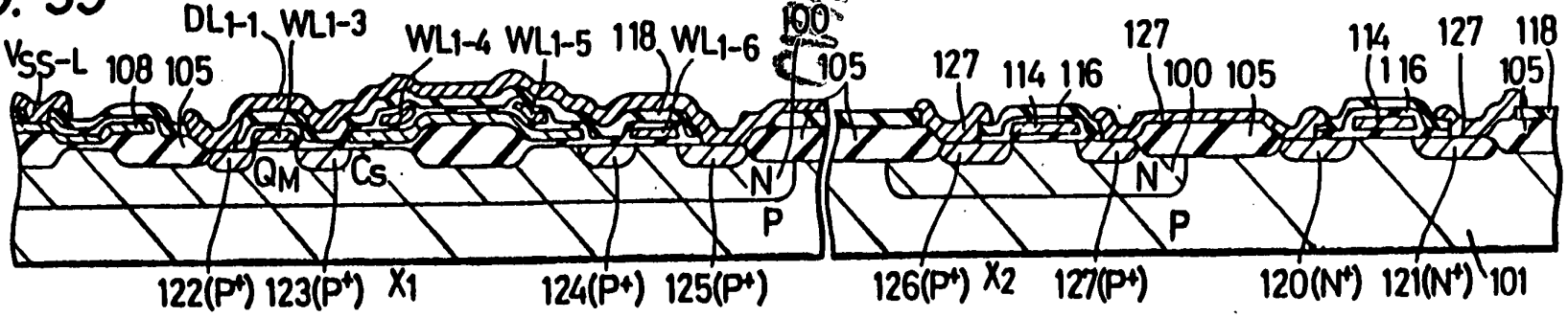


FIG. 35



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